Amendments to the Specification

Please amend the paragraph beginning at page 13, line 20 [more particularly, at page 14, line 13] of the Substitute Specification to read as follows:

Fig. 4 shows a second specific embodiment of the multiplexer circuit according to Fig. 2. A control circuit for controlling the bypass circuit comprises a sense circuit for sensing a voltage in the input channel. The sense circuit and the bypass circuit in combination form a bypass and sense circuit consisting of a sense path and a bypass path. In the bypass and sense circuit to V_{ss} the sense path comprises a PMOS transistor 130, 131 in series with an NMOS transistor 120, 121. The source of the PMOS transistor 130, 131 is connected to said first transmission gate FT_0, FT_1 and the source of the NMOS transistor 120, 121 is connected to ground level V_{ss}. The drain of the PMOS transistor 130, 131 is connected with the drain of the NMOS transistor 120, 121. The bypass path is formed of NMOS transistor 160, 161 the drain of which is connected with the output of said first transmission gate FT_0, FT_1 and the source of which is connected with V_{ss}. The gate of NMOS transistor 160, 161 is connected with the drains of the PMOS and NMOS transistors of the sense circuit. The driveability of NMOS transistor 120, 121 is very weak compared to the driveability of PMOS transistor 130, 131. For a channel that is switched off a voltage of $0.65V_{DD}$ is applied to gate of PMOS 130, 131. Both the sense path and the bypass path are switched off as long as the potential at node 70, 71 fulfils the condition $U70<0.65V_{DD}+|V_{THp}|$. When due to an over voltage at the input the voltage at node 70, 71 exceeds $\underline{U70>0.65V_{DD}+|V_{THp}|}$ ~~$U70<0.65V_{DD}+|V_{THp}|$~~ the sense path drives a small current to V_{ss}. Because of the big impedance of NMOS 120, 121 compared to the impedance of PMOS 130, 131 the gate voltage at the gate of bypass transistor NMOS 160, 161 increases very quickly so that this transistor changes very quickly to the conducting state. In this way a low impedance path to V_{ss} is installed when the voltage U70 is close to V_{DD}. The bypass and sense circuit to V_{ss} can be associated with an ideal switch that switches on as soon as U70 approximates V_{DD}.

Please amend the paragraph beginning at page 15, line 6 of the Substitute Specification to read as follows:

Measurements on real chips prove that a subthreshold current via closed FT_0 can occur also for valid input voltages $V_{SS}<Ul<V_{DD}$ dependent on the voltage drop between drain and source of FT_0. If this voltage drop is significant leakage is likely to occur due to the fact that the V_{DD} level in the chip (and at the gate of FT_0) is a little bit less than the v_{DD} level applied from externally and due to the big width of FT_0, which is necessary to achieve a small impedance if the input is active ADC input channel. The proposed bypass and sense circuits keep the voltage drop on FT_0 as small as possible and thus limit the subthreshold current into the pad. The reason is that both bypass and sense circuits are switched off for potentials U70 in the range $0.35V_{DD}-V_{THn}<U70<0.65V_{DD}+|V_{THp}|$,i.e. currents via FT_0 can only flow if one of the conditions $\underline{U70>0.65V_{DD}+|V_{THp}|}$ ~~$U70<0.65V_{DD}+|V_{THp}|$~~ or $U70<0.35V_{DD}-V_{THn}$ is fulfilled.